

AMENDMENTS TO THE SPECIFICATION

Immediately following the title, please add the following:

--CROSS REFERENCE TO RELATED APPLICATIONS

This application is a national phase patent application of PCT/GB04/03670 filed on August 27, 2004 which claims priority to United Kingdom Patent No. 0320167.0 filed on August 28, 2003.--

On page 1, Line 5, please insert: -- Background of the Invention—

On page 7 line 1 of the Specification please amend the first paragraph as follows:

--Two inverse-phased sin-wave voltage inputs are buffered by OPA 602 buffers and then connected to the non-inverting input of each AD844, where two capacitances C connected with the inverting inputs 2 of the OPA 602 buffers and two resistances r connected with the output 6 of a first AD844 chip can perfectly restore the Direct-Current (DC) components generated in the circuit and then cancel the DC offset at the current outputs. Eight AD844s constitute 4 pairs of two-output VCCSs.

Two inverting inputs of each pair of AD844s are ~~cascaded~~ connected together with a current- setting resistor R. The positive and negative current outputs of each pair are summed together to form larger current outputs. The total output currents can be estimated using the following function:--

On page 8, beginning with line 30 please amend the paragraph as follows:

--The coupling circuits, as shown in Figure 10, are made of a number of voltage buffers IC1 and passive components C1R1R2R3 to provide a wide bandwidth and fast settling ac-coupling interface, as well as a dc bypass to the dc current bias of the programmable gain amplifier (PGA). The input can be configured in either the single or the differential input mode. Only the differential mode is illustrated in Figure 10 for the use of the adjacent measurement strategy in electrical impedance tomography, where $R1=R3$ and $R1$ is much smaller than $R2$. Therefore, $R2, C1$ dominate the bandwidth of the coupling, $R1$ and $R3$ provide a DC bypass to the DC current offset of PGA but the responding speed is fast since the transient time is dominated by $R1$ or $R3$.--

On page 9, beginning with line 17 please amend the paragraph as follows:

--Figure 11 is the circuit used in the improved system to realize the over-current-zero switching technique. Two inverse-phased currents I^+ & I^- are connected to the common inputs of two multiplexers U1 & U2 respectively. The multiplexers may be MAX306 chips. 16 electrodes mounted in one sensing plane are connected to the 16 output channels (CH[0:15]) of each multiplexer U1,U2. Channel selection is together controlled by DSP command and a synchronize signal, SYN_SIN. SYN_SIN is a square-wave signal, which has the same over-zero point with two current signals I^+ & I^- . When DSP send out a switching command, an 8-bits data (each multiplexer is controlled by 4-bits data), ED[0:7], is written into the first flip-flop, U3 via inputs D1-D8. This data is later written into the second flip-flop, ~~U4~~, via outputs Q1-Q8 of U3 into inputs D1-D8 of U4 by the next rising edge of SYN_SIN, and then make the two multiplexers U1,U2 switch to other channels. A D-type flip-flop, U5A, is used in this circuit to prevent writing data into U4 before the data has been set-up at the output of U3. Flip-Flops U3, U4 may be MM74HC574 flip-flops and flip-flop U5 may be a MM74HL574A flip-flop.--